REMARKS

The acceptance of the formal drawings filed on June 6, 2006 is noted with appreciation.

The indication of withdrawal of the requirement for restriction is also noted with appreciation.

The specification has been amended in two locations: to insert a general reference to element 35 in Figure 2 (which was inadvertently omitted from the specification as filed); and to fill in the appropriate serial numbers where referenced. The specification has also been amended throughout for various editorial revisions. As these amendments are minor and non-substantive in nature, it is respectfully submitted that no new matter has been introduced.

Claims 1 - 20 remain active in this application. Claims 1 and 14 have been amended to clarify and emphasize the novel features of the invention. In particular, that the diffusion rate is *selectively* modified in both *lateral and vertical directions* in a region of semiconductor material *adjacent to the boundary* and *comparable to a diffusion rate of another impurity*. Support for this amendment can be found throughout the specification, particularly at paragraphs 0027-0028 and Figures 3A and 3B, as well as in the Abstract, in the application as published. No new matter has been introduced.

Claims 1-6, 14-18 and 20 have been rejected under 35 U.S.C. §102 as being anticipated by U.S. Patent 5,525,529 to Guldi. Claims 7-12 and 19 have been rejected under 35 U.S.C. §103 as being unpatentable over Guldi in view of U.S. Patent 6,159,813 to Ahmad. Claim 13 has been rejected under 35 U.S.C. §103 as being unpatentable over Guldi in view of U.S. Patent 6,882,025 to Yeo. These grounds of rejection are respectfully traversed particularly in view of the amendments above and remarks below.

The present invention is directed to modifying the diffusion rate of boron, or other impurities, in selected regions of a semiconductor material to approximate lower diffusion rates of other impurities. This is achieved by *selectively* reducing the diffusion rate at the edge of a gate structure with a film to apply stress to an *adjacent underlying region of the semiconductor* (see paragraph 0027-0028). As shown in Figure 3B, after annealing to activate the implanted impurities, diffusion 50 under the

gate 14 is significantly reduced in both lateral and vertical directions as compared to the diffusion of Figure 3A. Known diffusion rate modification techniques result in inadequate reduction of the diffusion rate of boron and allow it to diffuse over a greater distance. This results in many problems, such as causing the tip of the impurity region of extension implants to spread under the transistor gate, thus shortening the channel further increasing gate capacitance and increasing the junction depth within the silicon, and compromising a shallow channel geometry that allows the channel conductivity to be suitably controlled at low gate threshold voltages. Thus, there is a trade-off in the prior art between low resistance extensions and source/drain regions which require a high temperature activation annealing process and shallow junctions to maintain suitable switching thresholds and avoid undesirable roll-off effects (e.g. a reduction of switching threshold with reduction of channel length) which can lead to unacceptably low switching thresholds at short channel lengths. By providing a technique and structure for localized application of compressive stress, the claimed invention selectively reduces the boron diffusion rate at the edge of a pFET gate using a structure comprising a stressed film to apply stress to an adjacent underlying region of semiconductor material to reduce the diffusion rate of extension implants of pFET's to be comparable to arsenic/phosphorus implants in nFET's while allowing normal diffusion rate of boron in halo implants of nFET's . None of the cited references, either alone or in combination, teach or suggest the meritorious features of the claimed invention.

Contrary to the assertions made by the Examiner, the principal reference relied upon, Guldi, does not teach a method or structure for *localized* application of compressive stress. In fact, the Guldi disclosure does not even mention the terms "compressive" or "compress." Rather, the technique disclosed in Guldi is principally directed to applying films of different chemical compositions to semiconductor regions in order to reduce dopant diffusion by reduction of interstitial silicon. It appears that a chemical-configured blocking layer is provided along the semiconductor body so as to overlie the source/drain and depress the concentration of interstitial silicon or vacancies in the underlying source/drain in accordance with the diffusion mechanism of the selected dopant. Interstitial sites or vacancies in the source/drain regions are suppressed by *adjusting the chemical composition* of the overlying blocking layer. Thus, Guldi clearly teaches away from the claimed invention which does not utilize adjustments in chemical compositions to achieve its

meritorious effects. That is, Guldi uses adjustments of chemical concentration in the lattice structure for control of diffusion rate in a manner which does not appear to be localized or selective between impurities. In fact, the only mention of a stressed film (58 as pointed out by the Examiner) is disclosed as supplementary to the principal effects of silicon deficiency as well as appearing to be stressed only during annealing. That is, *Guldi does not recognize that boron diffusion rates can be made comparable much lower diffusion rates of other impurities by a stressed film applied at a boundary defined by a structure.*

Rather, as discussed at paragraph 0027, and shown in Figures 2-3B, *localized* application of a tensile film that develops a compressive force in the semiconductor material directly underlying the tensile film will result in the opposite sign of the stress in adjacent areas, and vice-versa, as well as tensile stress in a region closely adjacent to the boundary. In other words, localized application of compressive stress in a region of semiconductor material will be accompanied by an adjacent region of tensile stress (see regions 110 and 120 in Figure 2). Localization is achieved by defining a boundary with a structure (e.g., gate structure) on a surface of the semiconductor material. Thus, the effects of localized application of stressed film modifies the impurity diffusion rate as shown in Figures 3A-3B *without* having to adjust chemical compositions as in Guldi. These features are clearly disclosed in claim 1, as amended,:

> A method for *selectively* modifying a diffusion rate of an impurity . . .
> *defining a boundary with a structure* on a surface . . .
> applying a stressed film over said structure and said surface *at said boundary* . . .
> wherein said diffusion rate of said impurity is *selectively* modified *in both lateral and vertical directions* in a region of said semiconductor material *adjacent to said boundary* after said applying step to be *comparable to a diffusion rate of another impurity.*

and claim 14, as amended:

> a structure on a surface on said body of semiconductor material and *forming a boundary with said structure*, and

> a stressed film *extending over said structure and said boundary*, wherein when said intermediate structure is annealed to activate said boron and arsenic impurities, a diffusion rate of said boron impurities is *selectively* modified *in both lateral and vertical directions in a region of said semiconductor material adjacent to said boundary comparable to a diffusion rate of another impurity*.

Further, these novel features are clearly recited in independent claim 19:

> ... wherein a *boron diffusion concentration profile from extension implants* in said pFET *corresponds to a lower boron diffusion rate than a boron diffusion rate corresponding to a boron diffusion concentration profile from a boron halo implant* in said nFET.

and claim 20:

> ... wherein a *boron concentration profile of said extension region in a lateral direction differs from a boron concentration profile in a vertical direction.*

Thus, it is clearly shown that Guldi does not, and cannot, answer the explicit recitations of the claims, as amended, since Guldi neither anticipates nor renders obvious the meritorious features of the claimed invention.

Neither of the remaining references cited by the Examiner answer the deficiencies of Guldi, admitted or otherwise. Ahmad, cited for teaching implanting halo impurities, teaches nothing more than what is discussed in the application pertaining to problems with the prior art. In particular, Ahmad addresses implanting a boron halo to optimize concentration of p-type charge carriers. However, as discussed in the application, because of the high diffusion rate of boron in halo implants, the high diffusivity prevents use of extremely narrow spacers for self-aligned source/drain implants which are important to maintaining a low external resistance for the transistor while a larger spacer also tends to increase overall size of the transistor. As such, Ahmad teaches away from the claimed invention. In fact, it would be counterintuitive to one skilled in the art to combine a reference directed to

applying films of different chemical configurations to semiconductor regions in order to reduce dopant diffusion (Guldi) with a reference that side-steps any sort of diffusion rate control because an impurity is implanted later in processing of a sub-half-micron MOSFET (see column 4, lines 43-62 in Ahmad). Thus, even if properly combinable, the combination of Guldi and Ahmad would still not teach the claimed invention, as amended, since neither reference teach or suggest selective modification of a diffusion rate in a region adjacent to a boundary defined with a structure.

Yeo, cited for teaching a stressed film is a tensile film, does indicate that one of the disclosed films has an associated intrinsic tensile stress. However, as shown in Figures 4a-4b, the film referenced in Yeo as having an intrinsic tensile stress, the silicon nitride film 216, lines *trench isolation structures* 214. As such, Yeo cannot be used in combination with Guldi to reject any claim in the present invention because the claims specifically recite applying a stressed film over a structure *on a surface* of semiconductor material. Further, the combination would still not teach the claimed invention, as amended, since neither reference teaches or suggests selective modification of a diffusion rate in a region adjacent to a boundary defined with a structure. While Guldi may suggest some supplemental diffusion rate modification using a stressed film, it does not lead to an expectation of selective modification between structures, approximating a diffusion rate of another impurity using only applied stress or an expectation of beneficial adjustment of diffusion in both lateral and vertical directions.

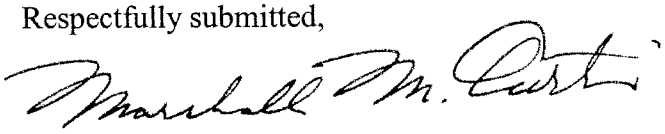
In summary, the grounds of rejection asserted in the office action are in error in regard to the claims as currently rejected or now amended since the references cited by the Examiner does not teach or suggest the novel features of the claimed invention, either as originally filed or as currently amended. For these reasons, it is respectfully submitted that the level or ordinary skill in the art determinable from the references relied upon is clearly insufficient to support a prima facie demonstration that any claim in the application is anticipated or obvious. Therefore, it is respectfully requested that the grounds of rejection be withdrawn and claims 1-20 be allowed.

Since all requirements contained in the outstanding official action have been fully answered and shown to be in error and/or inapplicable to the claims, it is respectfully submitted that reconsideration is now in order under the provisions of 37 C.F.R. §1.111(b) and such reconsideration is respectfully requested. Upon reconsideration, it is also respectfully submitted that this application is in condition

for allowance and such action is therefore respectfully requested.

If an extension of time is required for this response to be considered as being timely filed, a conditional petition is hereby made for such extension of time. Please charge any deficiencies in fees and credit any overpayment of fees to Deposit Account No. 09-0458 of International Business Machines Corp. (East Fishkill).

Respectfully submitted,



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Annotated Marked-Up Drawing

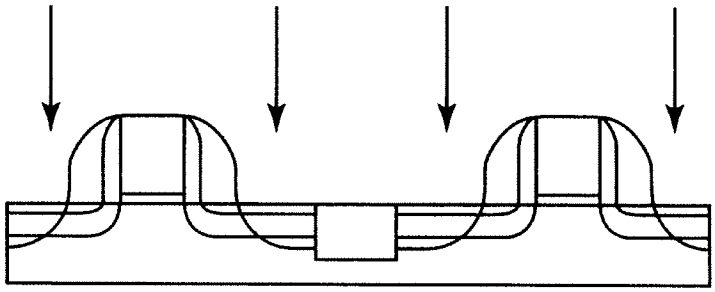

FIGURE 7

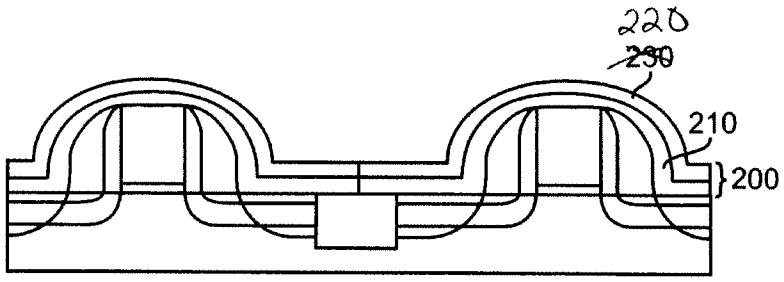

FIGURE 8

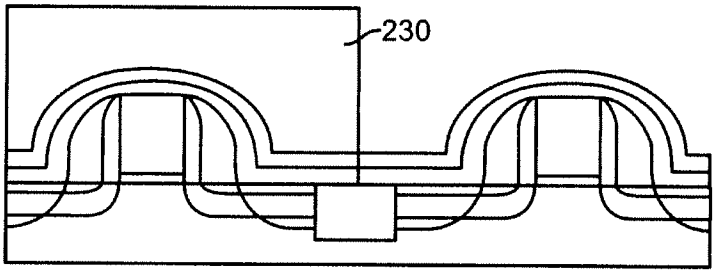

FIGURE 9